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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,424	09/18/2001	Fuji Yang	LARSSON 26-13-2	9474

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EXAMINER	
AHN, SAM K	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,424	YANG ET AL.	
	Examiner	Art Unit	
	Sam K. Ahn	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-18,20-29 and 31-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-18,21-29,32 and 33* is/are rejected.

7)☒ Claim(s) *9,20 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3,10,12-14,21,23-25 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shastri USP 6,552,619 B2 (cited previously) in view of Arkhipkin et al. US 6,018,547 (Arkhipkin) and Ishizu USP 5,651,031 (cited previously).

   Regarding claims 1,12 and 23, Shastri discloses a multi-channel serdes receiver (see Fig.1 in an integrated circuit, note col.1, line 19-20 inherently comprising a substrate and plurality of circuit layers), comprising: a central frequency synthesizer (2); and a plurality of channel-specific receivers (CRC0 ~ CRCn) coupled to said central frequency synthesizer, each of said plurality of channel-specific receivers including a clock recovery circuit having a phase detector (3) and a phase interpolator (6, and note col.15, lines 41-53, further shown as 70 in Fig.29), said clock recovery circuit coupling said phase detector and said central frequency synthesizer (as illustrated in Fig.1).

   However, Shastri does not explicitly teach the receiver including integrators and latches configured to perform demultiplexing operation of said data signal.

Arkhipkin teaches a receiver (see Fig.2c) including integrators (or accumulators, 286a,286b,288a,288b) and latches (290a,292a,292b and 290b) configured to perform a demultiplexing operation (outputting four outputs from two input, note col.2, lines 52-60). Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Arkhipkin of the integrators and latches in the receiver in the plurality of receivers of Shastri for the purpose of integrating one slot length of the incoming values, as taught by Ishizu (note col.2, lines 2-4), thus the system may calculate the phase of incoming signal compensating for any jitters that may cause undesirable results in phase computation. Furthermore, the system may select between the different paths (output of the latches (290a,292a,292b and 290b) by enabling and disabling the latches as desired.

Regarding claims 2,3,13,14,24 and 25, Shastri further teaches wherein said central frequency synthesizer (2) includes a voltage-controlled oscillator (VCO) and is a phase-locked loop (PLL), (note col.19, lines 30-35 wherein clocks are generated by a VCO in a PLL).

Regarding claims 4,15 and 26, Arkhipkin further teaches wherein said integrators are two integrators (286a,288a) configured to perform a first 1:2 demultiplexing operation of said data signal.

Regarding claims 10,21 and 32, Shastri further teaches a clock generation circuit (72a ~ 72d in Fig.29) coupled to said phase interpolator (6 in Fig.1 or 70 in Fig.29) and configured to generate a plurality of clock signals (RCKN, RCK, QRCKN, QRCK).

2. Claims 5,16 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shastri USP 6,552,619 B2 (cited previously) in view of Ishizu USP 5,651,031 and Arkhipkin et al. US 6,018,547 (Arkhipkin) and in further view of Hegeler USP 5,457,423 (cited previously).

   Regarding claims 5,16 and 27, Shastri in view of Arkhipkin and Ishizu teach all subject matter claimed, as applied to claim 4,15 or 26. However, Shastri in view of Arkhipkin and Ishizu do not explicitly teach wherein the integrating filter performs an integrate-and-dump function. Hegeler teaches wherein a filter is coupled to an integrate-and-dump circuit (see 4,5 in Fig.1) Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify the system to couple the integrate-and-dump circuit to the filter for the purpose of removing any noise and fading, as taught and supported by Shahriary (note col.2, lines 23-29). Thus, the combination of the two elements may be capable of functioning the limitation recited.

3. Claims 6,17 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shastri USP 6,552,619 B2 (cited previously) in view of Arkhipkin et al. US 6,018,547

(Arkhipkin) and Ishizu USP 5,651,031 (cited previously) and in further view of Perino et al. USP 6,687,319 B1 (Perino, cited previously).

Regarding claims 6,17 and 28, Shastri does not explicitly teach wherein the clock recovery circuit comprises a delay-locked loop clock and data recovery circuit. Perino teaches devices (2-4 in Fig.3) using a DLL clock (note col.12, lines 31-34, as is well-known), and further teaches wherein devices comprise data recovery circuit (see 46 in Fig.33). Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify Shastri's clock recovery circuit to be incorporated in the devices, taught by Perino comprising the DLL clock and the data recovery circuit for the purpose of recovering not only the clock signal but data signal as well, since noise and error may also affect the data signal.

4. Claims 7,18 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Shastri USP 6,552,619 B2 (cited previously) in view of Arkhipkin et al. US 6,018,547 (Arkhipkin) and Ishizu USP 5,651,031 (cited previously) and in further view of Brekelmans et al. USP 6,795,695 B1 (Brekelmans, cited previously).

Regarding claims 7,18 and 29, Shastri further teaches wherein said central frequency synthesizer (2) providing 16 phases (see Fig.4) wherein the 16 phases, however, does not explicitly teach providing in-phase and quadrature-phase clock signals.

However, does not explicitly teach wherein the central frequency synthesizer provides the in-phase and quadrature-phase clock signals.

Brekelmans teaches (see Fig.7a) central frequency synthesizer (FRE) providing the in-phase and quadrature-phase clock signals (note col.8, lines 5-7). Therefore, it would have been obvious to one skilled in the art at the time of the invention to transmit two different types of clocks by the central frequency synthesizer for the purpose of having different functions for each of the clocks, as taught by Brekelmans (note col.8, lines 1-12).

5. Claims 11,22 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shastri USP 6,552,619 B2 (cited previously) in view of Arkhipkin et al. US 6,018,547 (Arkhipkin) and Ishizu USP 5,651,031 (cited previously) and in further view of Perez USP 5,726,596 (cited previously).

Regarding claims 11,22 and 33, Shastri teaches all subject matter claimed, as applied to claim 10,21 or 32. However, Shastri does not explicitly teach at least one synchronizer configured to reduce skew between said plurality of clock signals. Perez teaches clock distribution system comprising synchronizer circuit (410,420 in Fig.4). Therefore, it would have been obvious to one skilled in the art at the time of the invention to couple Perez's synchronizer circuit to the output of Shastri's 72a~72d elements for the purpose of minimizing skew in the clock signals, as taught by Perez (note col.6, lines 1-8).

Allowable Subject Matter

6. Claims 9,20 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and overcome the claim objections.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Ahn whose telephone number is (571) 272-3044. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sam K. Ahn
1/22/06

YOUNG T. TSE
PRIMARY EXAMINER